Junhyeok Park

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Research Interests

Memory System: Researching architectural and system-level support for scalable solutions in heterogeneous computing.

- Developing unified virtual memory systems for efficient address space management across CPU, GPU, and NPU.
- Optimizing cache hierarchy and prefetching strategies.
- Enabling efficient inter-processor data transfer to reduce communication overhead.

GPUs: GPU micro-architecture and system design for monolithic and large-scale multi-chip GPUs

- Optimizing GPU execution paths to improve data locality and memory access efficiency.
- Exploring scalable multi-chip GPU systems for massive parallelism.

Education

Sungkyunkwan University, Korea   Mar 2023 - Feb 2025
Master Course in Electrical and Computer Engineering

- Advisor: Prof. Seokin Hong

Sungkyunkwan University, Korea   Mar 2017 - Feb 2023
Bachelor of Engineering in Electronic and Electrical Engineering

- **Summa Cum Laude**

Professional Experience

Electronics and Telecommunications Research Institute (ETRI), Korea   Jun 2025 – Jun 2026
Researcher (Pre-doctoral)

- Developing a system to accelerate LLM inference on heterogeneous computing platforms.

Publications

1st Author

- **Leveraging Chiplet-Locality for Efficient Memory Mapping in Multi-Chip Module GPUs**
  Junhyeok Park, Sungbin Jang, Osang Kwon, Yongho Lee, and Seokin Hong
  58th IEEE/ACM International Symposium on Microarchitecture (MICRO'25)

- **A Case for Speculative Address Translation with Rapid Validation for GPUs**
  Junhyeok Park, Osang Kwon, Yongho Lee, Seongwook Kim, Gwangeun Byeon, Jihun Yoon, Prashant J. Nair, and Seokin Hong
  57th IEEE/ACM International Symposium on Microarchitecture (MICRO'24)
  Best Paper Nominee
  IEEE Micro Top Picks Honorable Mention

2nd Author

- **SoftWalker: Supporting Software Page Table Walk for Irregular GPU Applications**
  Sungbin Jang, *Junhyeok Park*, Yongho Lee, Osang Kwon, Donghyun Kim, Juyoung Seok, and Seokin Hong
  58th IEEE/ACM International Symposium on Microarchitecture (MICRO'25)

- **Rethinking Page Table Structure for Fast Address Translation in GPUs: A Fixed-Size Hashed Page Table**
  Sungbin Jang, *Junhyeok Park*, Osang Kwon, Yongho Lee, and Seokin Hong
  The 33rd International Conference on Parallel Architectures and Compilation Techniques (PACT'24)

3rd Author

- **Distributed Page Table: Harnessing Physical Memory as an Unbounded Hashed Page Table**
  Osang Kwon*, Yongho Lee*, *Junhyeok Park*, Sungbin Jang, Byungchul Tak, and Seokin Hong
  57th IEEE/ACM International Symposium on Microarchitecture (MICRO'24)

- **Don't Cache, Speculate!: Speculative Address Translation for Flash-based Storage Systems**
  Hyungjin Kim, Seongwook Kim, *Junhyeok Park*, Gwangeun Byeon, and Seokin Hong
  IEEE Access, 2025

Language Proficiency

TOEFL iBT: 100 / 120

Skills

Software Languages: C (Kernel modules), C++, Python
Hardware Languages: Verilog
Parallel Computing: CUDA, MPI
Profiling & Analysis Tools: Nsight, NVBit
Simulation Tools: gem5, GPGPU-sim, DRAMsim

Teaching Assistant

Fall   2022: C++ Programming
Spring 2023: Problem Solving Methodology (C programming)
Fall   2023: C++ Programming
Spring 2024: Parallel Computer Architecture and Programming (CUDA)
Fall   2024: Advanced Memory System

Honors and Awards

Academic Excellence Scholarship, Sungkyunkwan University	Spring 2018 - Fall 2022, 6 semesters
Graduate Academic Excellence Scholarship, Sungkyunkwan University	Spring 2023 - Spring 2024, 3 semesters
Outstanding Research Award, Sungkyunkwan University	Feb 2025